IN THE CLAIMS

Please cancel claim 31, 33, 35 and 37, and further amend the claims as indicated below.

1-15. (canceled)

16. (currently amended) Method to implement a column interleaving function, comprising ~~the steps of~~:

providing a number of memories equal to ~~the~~ a maximum number of columns in ~~the~~ said column interleaving function;

inputting a stream of data entities in a serial format into a shift register that shifts said data entities therethrough and reformats said data entities from said serial format into a parallel format;

writing said data entities ~~successively~~, in said parallel format, from said shift register into said memories ~~a memory, until all memories are completely filled or until all data entities are written~~;

performing selection and permutation on said memories; and

reading out said data entities in said permuted memories, in a memory-by-memory fashion.

17. (currently amended) Method as in claim 16, wherein ~~the step of~~ said writing ~~into a memory~~ is applied when said shift register is filled.

18. (previously presented) Method as in claim 16, wherein said data entities are logical ones and zeros.

19. (previously presented) Method as in claim 16, wherein said data entities are multiple bit words.

20. (previously presented) Method as in claim 16, wherein said data entities are three bit words.

21. (previously presented) Method as in claim 17, wherein said shift register is arranged to store each multiple bit word at one location in said memories.

22. (currently amended) Method as in claim 16, wherein ~~the~~ a number of columns used in ~~the~~ said column interleaving function is changed on the fly, and wherein said number of columns ~~not exceeding~~ does not exceed said maximum number of columns.

23. (currently amended) A module comprising:

a number of memories equal to ~~the~~ a maximum number of columns in a column interleaving function;

a shift register that receives a stream of data entities in a serial format, shifts said data entities therethrough, and reformats said data entities from said serial format into a parallel format; and

a controller that controls:

writing said data entities ~~successively~~, in said parallel format, from said shift register into ~~a memory~~ said memories~~, until all memories are completely filled or until all data entities are written~~;

selection and permutation on said memories; and

reading out said data entities in said permuted memories, in a memory-by-memory fashion.

24. (previously presented) A communication system device, comprising a module as in claim 23.

25. (previously presented) A spread-spectrum communication apparatus comprising a module as in claim 23.

26. (currently amended) An integrated circuit device comprising:

a number of memories equal to ~~the~~ a maximum number of columns in a column interleaving function;

a shift register that receives a stream of data entities in a serial format, shifts said data entities therethrough, and reformats said data entities from said serial format into a parallel format; and

a sub-circuit that controls:

writing said data entities ~~successively~~, in said parallel format, from said shift register into said memories ~~a memory, until all memories are completely filled or until all data entities are written~~;

selection and permutation on said memories; and

reading out said data entities in said permuted memories, in a memory-by-memory fashion.

27. (previously presented) A communication system device, comprising an integrated circuit device as in claim 26.

28. (previously presented) A spread-spectrum communication apparatus comprising an integrated circuit device as in claim 26.

29. (currently amended) A column interleaver, comprising:

a number of memories equal to ~~the~~ a maximum number of columns desired in ~~the~~ said column interleaver;

a shift register that receives a stream of data entities in a serial format, shifts said data entities therethrough, and reformats said data entities from said serial format into a parallel format; and

a module that controls (a) writing of said data entities, in said parallel format, from said shift register to said memories, and (b) column selection and permutation.

30. (canceled)

31. (canceled)

32. (currently amended) The module of claim 23, wherein said controller controls said writing to ~~occure~~ occur when said shift register is filled.

33. (canceled)

34. (currently amended) The integrated circuit device of claim 26, wherein said sub-circuit controls said writing to occur when said shift register is filled.

35. (canceled)

36. (previously presented) The column interleaver of claim 29, wherein said module controls said writing to occur when said shift register is filled.

37. (canceled)